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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,897	11/27/2001	Masayuki Fukumi	829-590	7681

7590 11/25/2003

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/993,897	FUKUMI, MASAYUKI	
	Examin r	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication app ars on th cover sheet with th c rr spondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be evaileble under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed efter SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified ebove, the maximum statutory period will epply end will expire SIX (6) MONTHS from the mailing date of this communicetion.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later then three months efter the meiling dete of this communicetion, even if timely filed, may reduce eny earned patent term edjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 15* is/are allowed.

6)☒ Claim(s) *1,2,7-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *08192003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7, 9-11, 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoigawa et al. U.S. Patent 5,946,549 A.

Itoigawa et al. discloses a semiconductor substrate device, comprising; a first semiconductor substrate 22 including a concave-convex surface, the concave-convex surface comprising a convex portion including a top surface; a second semiconductor substrate 25 having a non-glass thin film silicon insulator (24a, 24b) on a surface thereof, wherein the first semiconductor substrate 22 and the second semiconductor substrate 25 are together so that the top surface of the convex portion of the concave-convex surface of the first semiconductor substrate 22 and the thin film insulator provided on the surface of the second semiconductor substrate 25 contact each other, wherein the thin film silicon insulator is the only circuit or device element located therebetween, to form a cavity in the semiconductor substrate device (see figure 9D). While the drawings show steps for producing a single pressure sensor, Itoigawa et al. also discloses producing a plurality of pressure sensors on a single wafer, therefore forming a two dimensional array of cavities in the semiconductor substrate device

defined by a plurality of convex portions formed at equal intervals (see column 5, lines 38-42).

As to the language on claims 14 and 16 "wherein the two-dimensional array of cavities serve as respective low dielectric constant portions so that parasitic capacitance generated between the first substrate and circuit elements on the second substrate is reduced", applicant should note that this is merely result language which can not be relied upon to define over Itoigawa et al., since Itoigawa et al. recited all of the claimed elements and their recited relationships. Moreover the examiner will presume that the recited results are inherent in Itoigawa et al., since all of the claimed elements and the relationship therebetween are met by Itoigawa et al..

3. Claims 1, 2, 8, 10, 11, 12 and 14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fujii et al. U.S. Patent 4,975,390 A.

Fujii et al. discloses a semiconductor substrate device, comprising; a first semiconductor substrate 1 including a concave-convex surface; the concave- convex surface comprising a convex portion including a top surface and a plurality of convex portions formed at equal intervals wherein widths of the concave portions narrows as the depth of the concave portions increases (see figure 9a); a second semiconductor substrate 4 having a non-glass thin film silicon oxide insulator 5 on a surface thereof, the insulator 5 having less thickness than the substrate 4; wherein the first semiconductor substrate 1 and the second semiconductor substrate 4 are brought together so that the top surface of the convex portion of the concave-convex surface of the first semiconductor substrate 1 and the thin film insulator 5 provided on the surface

of the second semiconductor substrate 4 contact each other with no circuit or device element located therebetween, to form a two-dimensional array of cavities in the semiconductor substrate device (see figure 9c).

As to the language on claim 14 "wherein the two-dimensional array of cavities serve as respective low dielectric constant portions so that parasitic capacitance generated between the first substrate and circuit elements on the second substrate is reduced", applicant should note that this is merely result language which can not be relied upon to define over Fujii et al., since Fujii et al. recited all of the claimed elements and their recited relationships. Moreover the examiner will presume that the recited results are inherent in Fujii et al., since all of the claimed elements and the relationship therebetween are met by Fujii et al..

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Itoigawa et al. U.S. Patent 5,946,549 A.

Itoigawa et al. is applied as above but lacks anticipation on disclosing the thin film silicon layer being thinner than the second semiconductor substrate, however, selecting an optimum thickness value for the thin film silicon layer, e.g., thinner than the second semiconductor substrate, is only considered to be routine optimization of the device disclosed by Itoigawa et al. since Itoigawa et al. already discloses a thin film insulating layer, therefore optimizing the invention disclosed in Itoigawa et al. by changing the thin film thickness to a desire thickness involve only routine skills in the art and it would have been obvious to a person having ordinary skills in the art at the time the invention was made.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 2 and 6-13 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

9. Claims 6 and 15 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination failed to anticipate or render obvious the limitations of having a second semiconductor substrate on which a thin film oxide is provided being implanted with hydrogen ions and wherein bonding the second semiconductor substrate to a first semiconductor substrate having a concave convex surface forms a two dimensional array of cavities with no circuit or device element between the oxide film and the first substrate as required by claim 6.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen et al. discloses a semiconductor substrate device having two semiconductor substrates bonded by an insulating layer to form a two-dimensional array of cavities with no circuit or device element therebetween. Delgado et al. and

Koshino et al. disclose semiconductor substrate devices having semiconductor substrates bonded by insulating layers to form two-dimensional array of cavities.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR